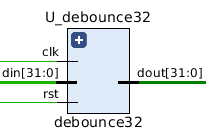
Debounce

# 1.1 implementation



Signal list:

in clk: clock signal

in rst: reset signal, active-high

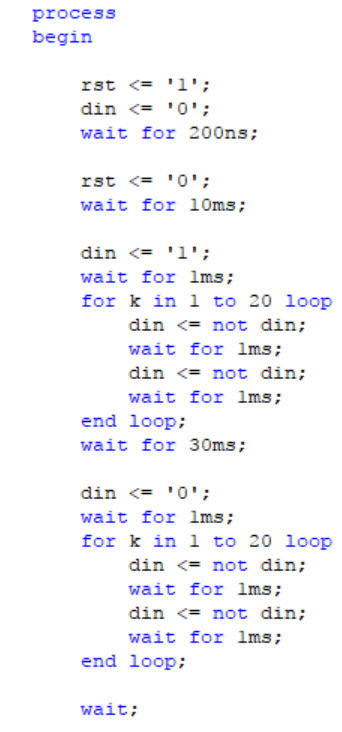
in din: input data

out dout: output data

This is a unit for input debouncing. It uses 4 states machine to achieve debounce. It gets the data only when the state is idle. When pressing and releasing are not stable, the machine will keep in the “press” and “release” state and will not send the signal to output.

# 1.2 Testbench

For this unit, we only need to set the din to ‘0’ and ‘1’ to check if it is working.



# 1.3 functional simulation

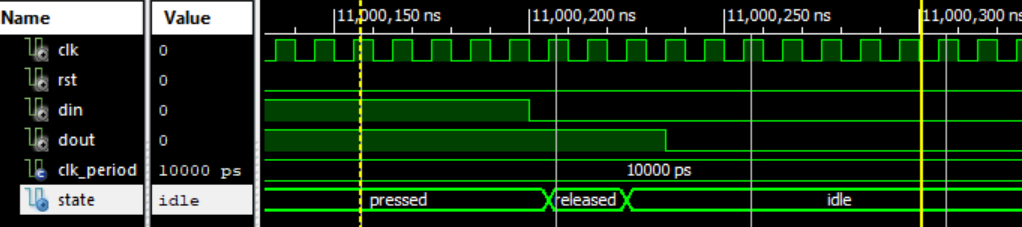


Figure 1.3.1 test case press to release

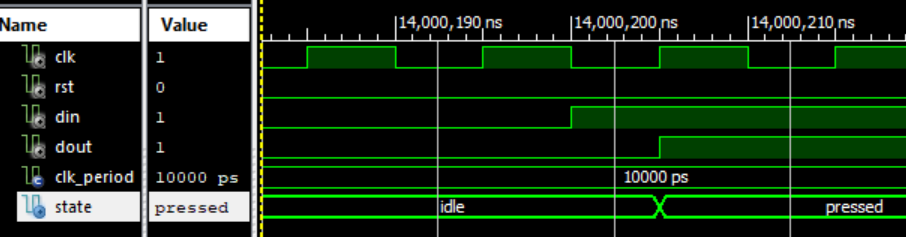


Figure 1.3.2 test case release to press

# 1.4 timing simulation

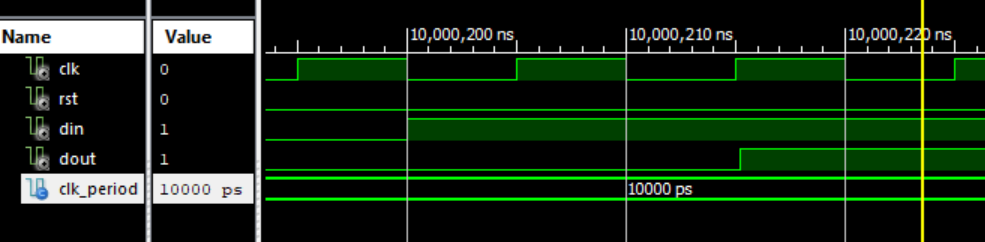


Figure 1.3.1 test case press to release

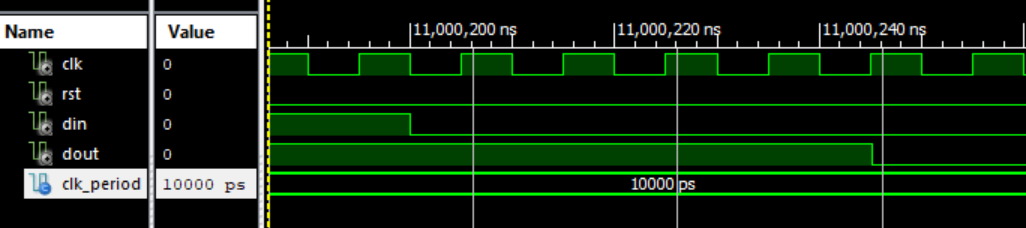


Figure 1.3.2 test case release to press

# 1.5 Timing analysis

|  |  |
| --- | --- |
| Critical path delay | 4.3 ns |
| Highest frequency | 233 MHz |